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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,965	08/04/2003	Haihong Wang	H1178	4486

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,965	WANG ET AL.	
	Examiner	Art Unit	
	Hung K. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/4/03 & 10/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Invention of Group I, claims 1-9 and 15-20, in the reply filed on 08/02/04 is acknowledged.

Claims 10-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 08/02/04.

Claim Objections

2. Claims 9 and 19 are objected to because of the following informalities:

In claim 9, line 1, "later" should be changed to "layer" for clarity.

In claim 19, line 2, "have" should be changed to "has" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-9, 15-18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hisamoto et al. (IEEE 2000, of record).

Hisamoto et al. discloses, as shown in Figures 1, 2 and 5, a semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

a source region formed on the insulting layer adjacent a first side of the fin;

a drain region formed on the insulating layer adjacent a second side of the fin opposite the first side, wherein the source and drain regions have a greater thickness than the fin.

With regard to claim 2, Hisamoto et al. discloses the fin has a thickness of 500 Å (within ranging from about 500 Å to about 800 Å) in a channel region of the semiconductor device.

With regard to claim 4, Hisamoto et al. discloses the fin has a width of 100 Å or 200 Å (within ranging from about 50 Å to about 200 Å) in a channel region of the semiconductor device.

With regard to claim 5, Hisamoto et al. discloses the device further comprising:

a gate formed over a top surface of the fin in a channel region of the semiconductor device.

With regard to claim 6, Hisamoto et al. discloses the gate comprises a first gate disposed on a third side of the fin and a second gate disposed on a fourth side of the fin opposite the third side.

With regard to claim 7, Hisamoto et al. discloses the device further comprising:

at least one dielectric layer formed over a top surface of the fin.

With regard to claim 8, Hisamoto et al. discloses the device further comprising:

a gate formed over the at least one dielectric layer and being disposed on a third and fourth side of the fin.

With regard to claim 9, Hisamoto et al. discloses the insulating layer comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

With regard to claim 15, Hisamoto et al. discloses, as shown in Figures 1, 2 and 5, a semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end and a second end;

a source region formed adjacent the fist end of the conductive fin;

a drain region formed adjacent the second end of the conductive fin, wherein the source and drain regions have a greater thickness than the conductive fin in a channel region of the semiconductor device.

With regard to claim 16, Hisamoto et al. discloses the device further comprising:

a gate dielectric layer formed on the conductive fin in the channel region of the semiconductor device;

a gate formed over the gate dielectric layer.

With regard to claim 17, Hisamoto et al. discloses the gate comprises a fist gate electrode disposed on a firs side of the conductive fin and a second gate electrode disposed on a second side of the conducive fin opposite the first side.

With regard to claim 18, Hisamoto et al. discloses the conductive fin has a thickness of 500 Å (within ranging from about 500 Å to about 800 Å) and a width of 100 Å or 200 Å (within ranging from about 50 Å to about 200 Å) in a channel region of the semiconductor device.

With regard to claim 20, Hisamoto et al. discloses the source and drain regions are each at least about 200 Å thicker than the conductive fin in a channel region of the semiconductor device.

4. Claims 1-3, 5-9, 15-17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (IEEE 1999, of record).

Huang et al. discloses, as shown in Figures 1 and 10, a semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

a source region formed on the insulting layer adjacent a first side of the fin;

a drain region formed on the insulating layer adjacent a second side of the fin opposite the first side, wherein the source and drain regions have a greater thickness than the fin.

With regard to claim 2, Huang et al. discloses the fin has a thickness of 500 Å (within ranging from about 500 Å to about 800 Å) in a channel region of the semiconductor device.

With regard to claim 3, Huang et al. discloses the source region and drain region each has a thickness of 1000 Å (within ranging from about 700 Å to about 1000 Å).

With regard to claim 5, Huang et al. discloses the device further comprising:

a gate formed over a top surface of the fin in a channel region of the semiconductor device.

With regard to claim 6, Huang et al. discloses the gate comprises a first gate disposed on a third side of the fin and a second gate disposed on a fourth side of the fin opposite the third side.

With regard to claim 7, Huang et al. discloses the device further comprising:

at least one dielectric layer formed over a top surface of the fin.

With regard to claim 8, Huang et al. discloses the device further comprising:

a gate formed over the at least one dielectric layer and being disposed on a third and fourth side of the fin.

With regard to claim 9, Huang et al. discloses the insulating layer comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

With regard to claim 15, Huang et al. discloses, as shown in Figures 1 and 10, a semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end and a second end;

a source region formed adjacent the first end of the conductive fin;

a drain region formed adjacent the second end of the conductive fin, wherein the source and drain regions have a greater thickness than the conductive fin in a channel region of the semiconductor device.

With regard to claim 16, Huang et al. discloses the device further comprising:

a gate dielectric layer formed on the conductive fin in the channel region of the semiconductor device;

a gate formed over the gate dielectric layer.

With regard to claim 17, Huang et al. discloses the gate comprises a first gate electrode disposed on a firs side of the conductive fin and a second gate electrode disposed on a second side of the conducive fin opposite the first side.

With regard to claim 20, Huang et al. discloses the source and drain regions are each at least about 200 Å thicker than the conductive fin in a channel region of the semiconductor device.

5. Claims 1-3, 5-9, 15-17 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang et al. (IEEE 2001, of record).

Huang et al. discloses, as shown in Figures 1 and 8, a semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

a source region formed on the insulting layer adjacent a first side of the fin;

a drain region formed on the insulating layer adjacent a second side of the fin opposite the first side, wherein the source and drain regions have a greater thickness than the fin.

With regard to claim 2, Huang et al. discloses the fin has a thickness of 300 Å to 1500 Å (within ranging from about 500 Å to about 800 Å) in a channel region of the semiconductor device.

With regard to claim 3, Huang et al. discloses the source region and drain region each has a thickness of 1000 Å (within ranging from about 700 Å to about 1000 Å).

With regard to claim 5, Huang et al. discloses the device further comprising:

a gate formed over a top surface of the fin in a channel region of the semiconductor device.

With regard to claim 6, Huang et al. discloses the gate comprises a first gate disposed on a third side of the fin and a second gate disposed on a fourth side of the fin opposite the third side.

With regard to claim 7, Huang et al. discloses the device further comprising:

at least one dielectric layer formed over a top surface of the fin.

With regard to claim 8, Huang et al. discloses the device further comprising:

a gate formed over the at least one dielectric layer and being disposed on a third and fourth side of the fin.

With regard to claim 9, Huang et al. discloses the insulating layer comprises a buried oxide layer and the fin comprises at least one of silicon and germanium.

With regard to claim 15, Huang et al. discloses, as shown in Figures 1 and 10, a semiconductor device, comprising:

a substrate;

an insulating layer disposed on the substrate;

a conductive fin formed on the insulating layer, the conductive fin having a first end and a second end;

a source region formed adjacent the fist end of the conductive fin;

a drain region formed adjacent the second end of the conductive fin, wherein the source and drain regions have a greater thickness than the conductive fin in a channel region of the semiconductor device.

With regard to claim 16, Huang et al. discloses the device further comprising:

a gate dielectric layer formed on the conductive fin in the channel region of the semiconductor device;

a gate formed over the gate dielectric layer.

With regard to claim 17, Huang et al. discloses the gate comprises a first gate electrode disposed on a firs side of the conductive fin and a second gate electrode disposed on a second side of the conducive fin opposite the first side.

With regard to claim 20, Huang et al. discloses the source and drain regions are each at least about 200 Å thicker than the conductive fin in a channel region of the semiconductor device.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hisamoto et al. (IEEE 2000, of record).

Hisamoto et al. discloses the total source region and the drain region thickness is 4000 Å. Hisamoto et al. does not disclose the source region and the drain region each has a thickness ranging from about 700 Å to about 1000 Å. Although Hisamoto et al. do not teach the thickness of the source region and the drain region, as that claimed by Applicants, however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the source region and the drain region having a desired thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claims 4, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (IEEE 1999, of record) or Huang et al. (IEEE 2001, of record)

Huang et al. discloses the total source region and the drain region thickness is 1000 Å. Huang et al. does not disclose the conductive fin has a width as that claim by Applicants. Although Huang et al. do not teach the width of the conductive fin, however, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the source region and the drain region having a desired thickness, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

August 23, 2004

Hung Vu

Patent Examiner